Gate-tunable graphene-organic interface barrier for vertical transistor and logic inverter

Subir Parui, Mário Ribeiro, Ainhoa Atxabal, Kaushik Bairagi, Elisabetta Zuccatti, C. K. Safeer, Roger Llopis, Fèlix Casanova, and Luis E. Hueso

Citation: Appl. Phys. Lett. **113**, 153301 (2018); doi: 10.1063/1.5045497
View online: https://doi.org/10.1063/1.5045497
View Table of Contents: http://aip.scitation.org/toc/apl/113/15
Published by the American Institute of Physics

Gate-tunable graphene-organic interface barrier for vertical transistor and logic inverter

Subir Parui,[1,a),b)] Mário Ribeiro,[1,2,3] Ainhoa Atxabal,[1] Kaushik Bairagi,[1] Elisabetta Zuccatti,[1] C. K. Safeer,[1] Roger Llopis,[1] Fèlix Casanova,[1,4] and Luis E. Hueso[1,4,b)]
[1]*CIC nanoGUNE, 20018 Donostia-San Sebastian, Basque Country, Spain*
[2]*Center for Quantum Nanoscience, Institute for Basic Science (IBS), Seoul 03760, South Korea*
[3]*Department of Physics, Ewha Womans University, Seoul 03760, South Korea*
[4]*IKERBASQUE, Basque Foundation for Science, 48013 Bilbao, Basque Country, Spain*

(Received 20 June 2018; accepted 26 September 2018; published online 11 October 2018)

One of the key requirements for efficient organic-electronic devices is the creation of a negligible energy barrier for carrier injection at the metal-organic interface. Here, a graphene-organic interface with an almost negligible energy barrier is demonstrated in a high-performance hybrid heterojunction device. The gate-tunable current-voltage characteristics show that the electronic transport can be tuned from an interface-limited to a bulk-dominated regime by lowering the graphene-organic interface energy barrier. N-type transistors with a PTCDI-C8 organic thin film as an active layer provide an ON-OFF current ratio of $\sim 10^7$, while similar p-type transistors with a CuPc molecular layer reach an ON-OFF current ratio of $\sim 10^5$. Furthermore, logic inverters with standby current as low as ~ 1 pA are demonstrated using a combination of both n- and p-type transistors. *Published by AIP Publishing*. https://doi.org/10.1063/1.5045497

The integration of graphene-organic heterostructures into vertical high-performing transistors has become a promising route towards achieving compact and energy-efficient organic electronic devices.[1–3] In recent years, vertical devices have been actively sought for replacing conventional lateral organic thin film transistors, such as those used for bendable active matrix organic light emitting diodes, radio-frequency identification tags, and low-power electronics.[4–6] However, the existing vertical graphene-organic transistors still provide unacceptably large currents in their OFF-state, which make them unsuitable for low power applications and deliver poor ON-OFF ratios around four orders of magnitude.[7–11]

Organic electronics utilizes highly functional molecular materials in common electronic devices to electrically access their wide range of semiconducting properties. However, the presence of an energy barrier across the interface between the metal contact and the organic layer prevents the investigation of intrinsic charge transport properties of organic semiconductors and poses limitations towards optimized device performance.[12] A barrier-free contact to organic semiconducting channels is then a key step towards the development of high-performance organic devices,[13] which can be reached using the gate-tunability of the graphene-organic interface.[8,9]

In this work, taking advantage of the unique properties of graphene[14–16] in combination with organic molecules, we demonstrate high-performance vertical graphene-organic heterojunction transistors. Our approach presents a gate-tunable graphene-organic hybrid system in which both the Fermi level of graphene and the induced charge carriers in the organic material can be modulated by the electrostatic field to the extent that almost a barrier-free graphene-organic contact is achieved for a wide range of applied gate voltages. Thanks to the electrically transparent contacts, we further tune the carrier transport from an interface-limited to a bulk-dominated regime.

As a proof-of-concept, a vertical transistor has been fabricated with an organic n-channel of N,N′-dioctyl-3,4,9,10-perylene dicarboximide (PTCDI-C8) planar molecules and a graphene bottom electrode. It shows room temperature operation with a stable OFF-state current below 1 pA, an ON-state current of up to 1 μA (current density of ~ 100 A m^{-2}), and an ON-OFF current ratio of up to 10^7. The organic material under study has been selected taking into account that perylene diimides, the molecular family of PTCDI-C8, are good electron conductors due to their relatively large electron affinities. Simultaneously, we have also developed a p-type transistor with a CuPc organic layer that can provide an ON-OFF current ratio above 10^5 with an OFF-state current around ~ 1 pA. Furthermore, we integrate the different transistors into a more complex complementary logic inverter.

The vertical graphene-organic transistors are based on chemical vapor deposition (CVD)-grown graphene transferred onto a Si/SiO_2 substrate.[9,17] The CVD-graphene is lithographically patterned and etched by argon/oxygen plasma into several stripes, to which Ti/Au bilayers are deposited for electrical contacts. Each graphene stripe is used as the source (S) of the vertical transistor. A 200-nm-thick layer of either n-type PTCDI-C8 or p-type CuPc is evaporated onto the graphene stripes under ultra-high vacuum (UHV) conditions after an overnight *in-situ* annealing step at 250 °C. This *in-situ* annealing step minimizes the adsorbed water in the graphene device and provides a relatively inert surface for the growth of the organic layer. Finally, a 15-nm-thick Al film is thermally deposited on top of the molecular layer as the drain contact (D) (see supplementary material for further details).

[a)]Present address: IMEC, Kapeldreef 75, 3001 Leuven, Belgium and KU Leuven, Kasteelpark Arenberg 44, 3001 Leuven, Belgium
[b)]E-mail addresses: subirparui@gmail.com and l.hueso@nanogune.eu

In Fig. 1, we show the electrical transport studies of vertical n-type and p-type organic transistors. The graphene source electrodes used for the vertical transistors are hole-doped, which is consistent with our previous studies.[9,17] We first show the output characteristics (that is, the drain current versus the drain voltage) of the graphene/PTCDI-C8/Al transistor in Fig. 1(a). The experimental data at various V_G clearly show that the drain current increases with increasing positive gate potential, which demonstrates that electrons are the majority charge carriers and confirms the n-type nature of PTCDI-C8. The transistor exhibits a nearly symmetric drain current flow for several gate voltages, unlike in previous studies.[9,17] This fact suggests that the gate voltage actively modulates the number of induced charge carriers inside the organic channel, and thus, the overall conductivity increases. We understand that a similar behaviour would emerge if the gate voltage could modulate both the graphene/PTCDI-C8 and PTCDI-C8/Al interfaces simultaneously. However, we disregard such a possibility since a tunable energy barrier at the PTCDI-C8/Al interface is unlikely due to the large density of states of aluminium.[7] The presence of a small asymmetry in the I_D-V_D plots is explained by the tunable graphene/PTCDI-C8 interface energy barrier at large negative gate voltages. In order to further investigate the gate modulation, Fig. 1(b) shows the transfer characteristics (I_D-V_G curves) for the same device at several positive V_D. Overall, we observe a room-temperature ON-OFF current ratio reaching nearly seven orders of magnitude, which is a clear improvement from graphene-organic hybrid devices in the current literature [Fig. 1(c)].[10,18] Furthermore, the steady OFF-state current is below 1 pA, which is a suitable value for developing low power dissipative circuit elements.

Similarly, the electrical characteristics of a p-channel graphene/CuPc/Al transistor are shown in Figs. 1(d)–1(f), respectively. Figure 1(d) shows the output characteristics of the transistor. The overall drain current increases when the gate voltage changes from positive to negative polarity, confirming that holes are the majority charge carriers.[19] In this p-type device, we observe a nearly symmetric I_D-V_D plot only for intermediate gate voltages since the hole-doped graphene electrode and the Al top-contact for a p-type semiconductor make the hole-transport more complex than for the previous case. Nevertheless, the overall increase in I_D for both polarities of V_D with respect to the change in V_G indicates that there is also significant bulk-charge carrier modulation in the organic material. For large negative V_G, the back-diode characteristics (I_D is higher for $-V_D$ than $+V_D$) mark the presence of a rectifying energy barrier at the CuPc/Al interface, which arises due to a large mismatch between the highest occupied molecular orbital (HOMO) of CuPc [−5.2 eV (Ref. 3)] and the work function of Al (−4.0 eV). In this case, the device shows a room-temperature ON-OFF current ratio of five orders of magnitude with a steady OFF-state current of ∼1 pA.

In order to gain insights into the transport mechanisms, we investigate the temperature dependent transport characteristics of the n-type graphene/PTCDI-C8/Al diode. Figure 2(a)

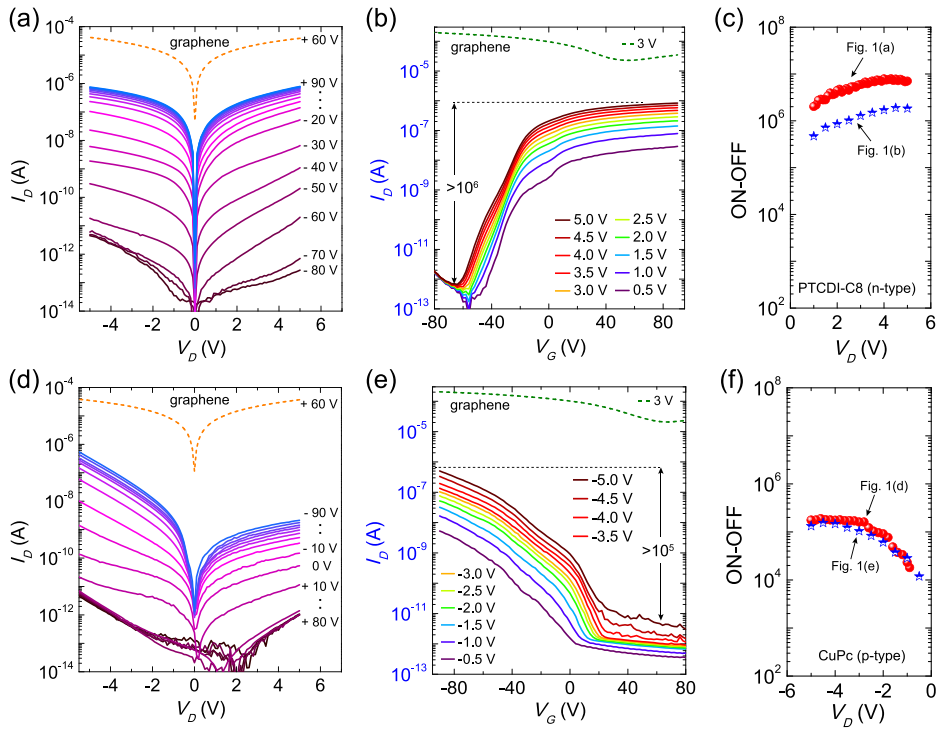

FIG. 1. (a) Drain current (I_D) as a function of drain–source voltage (V_D) at various gate-source voltages (V_G) for the n-channel graphene/PTCDI-C8/Al transistor. The dotted I_D-V_D plot represents the characteristics of the graphene-source electrode at $V_G = 60$ V (charge neutrality point). (b) Drain current measured at various positive drain-source voltages (reverse-bias for the n-channel diode) as a function of the gate voltage for the same n-type transistor. The doted I_D-V_G plot represents the transistor characteristics of the graphene electrode. (c) ON-OFF current ratio is calculated by dividing ON and OFF currents from (a) and also from (b) for positive drain voltages. (d) The I_D-V_D plots for the p-channel graphene/CuPc/Al transistor. (e) The I_D-V_G plots at various negative drain-source voltages (reverse-bias for the p-channel diode) as a function of the gate voltage for the same p-type transistor. (f) ON-OFF current ratio is calculated by dividing ON and OFF currents from (d) and also from (e) for negative drain-voltages.

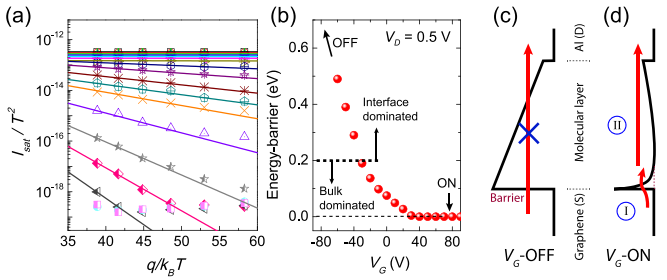

FIG. 2. (a) Temperature-dependent reverse-biased diode characteristics of the n-type graphene/PTCDI-C8/Al transistor. The saturation current is considered to be the drain current at $V_D = 0.5$ V. Then, I_{sat}/T^2 is plotted against q/k_BT and fitted exponential to extract the graphene-PTCDI effective interface energy barrier heights. (b) The graphene/PTCDI-C8 effective interface energy barrier height plotted as a function of the gate voltage. (c) Schematic illustration of the device operation. An applied negative V_G shifts the Fermi level in such a way that it increases the effective potential barrier and switches OFF the transistor. The arrow indicates the flow of charge carriers. (d) Sweeping V_G towards positive values increases the flow of electrons from the graphene bottom electrode to the Al top electrode due to significant reduction in the energy-barrier (process I) and simultaneously enhances the field-emission in the organic layer (process II). These mechanisms switch ON the transistor.

shows the drain current in the temperature range from 300 K to 200 K, at various values of V_G and at $V_D = 0.5$ V. We can approximately determine the graphene/PTCDI-C8 interface energy barrier height (φ_B) by applying the Richardson-Dushman thermionic emission theory[8,9]

$$I_{sat} = I_D(V_D = 0.5V) = AA^*T^2 \exp\left(-\frac{q\varphi_B}{k_BT}\right), \qquad (1)$$

where A is the junction area, A^* is the effective Richardson constant of PTCDI-C8, q is the elementary charge, k_B is the Boltzmann constant and T is the temperature. Figure 2(b) presents the variation of the extracted φ_B with respect to the applied gate-voltages. From Fig. 2(b), we can identify three different regimes of φ_B versus V_G variation: (i) a regime of effective zero interfacial energy barrier, (ii) a slow increase in the energy barrier of up to ~0.2 eV, and then (iii) a sharp increase above ~0.2 eV. In general, the transport mechanism in a vertical diode is considered to be bulk-dominated when the interface energy barrier is lower than ~0.2 eV (Refs. 20 and 21), and thus, from the plot in Fig. 2(b), we infer the transport regimes to be qualitatively different below and above such a boundary.[22,23] The carrier conduction in this transistor is actively bulk-dominated; however, a large effective interface energy barrier height allows switching OFF the device down to a stable current below 1 pA. Further transport analysis based on reverse-biased (i.e., the positive drain voltages) I_D-V_D characteristics can be found in the supplementary material.

Figures 2(c) and 2(d) display the schematic diagram of the device operation principle of the graphene-PTCDI-Al field-emission transistor. The applied bottom gate voltage not only shifts the Fermi level (E_F) of graphene but also changes the carrier concentration in the organic channel above the electrode due to the weak screening of graphene.[9] For an n-type semiconducting channel, a large negative gate voltage increases the E_F of graphene with respect to the vacuum level, raising the effective energy barrier height at the graphene-organic interface. At the same time, the negative gate voltage depletes the available charge carriers inside the n-type organic semiconductor. In this scenario, the electrons cannot flow from graphene to Al through the organic layer, and the "OFF" state is achieved in the transistor operation as depicted in Fig. 2(c). By contrast, a positive gate voltage shifts the graphene Fermi level closer to the lowest unoccupied molecular orbital (LUMO) level, reduces the interface energy barrier height, and induces mobile electrons inside the n-type organic channel, which will cause the "ON" state of the transistor [see Fig. 2(d)]. For the case in which electrons are present in the transport channel, the shape of the barrier becomes very thin and allows tunneling at the interface (process I) and field-emission (process II) inside the organic material. In the best possible scenario, the electrons will be able to flow from graphene to the organic molecular layer without facing any interface barrier, and the transport will be fully controlled by the bulk of the organic film.

We can now tackle an integrated device functionality based on the hybrid graphene-organic heterostructures and focus on two diverse complementary inverters.[24] Figure 3(a) shows the inverter operation using a single n-type transistor connected with a load resistance of 1.5 GΩ. The circuit diagram for this inverter is displayed in the inset of the figure. The top panel of Fig. 3(a) presents the inverter voltage transfer characteristics at supply voltages (V_{DD}) of 1, 3, and 5 V. The output voltages (V_{OUT}) remain equal to the applied V_{DD} values at negative input voltages (V_{IN}), and they change to 0 V by sweeping the input voltage (V_{IN}) from negative towards positive values. However, if we follow the supply current (I_{DD}) in the bottom panel of Fig. 3(a), we observe that it drives a very low current of ~1 pA before the inversion and a steady current of ~1 nA after the inversion. In order to minimize the large steady current dissipation, we

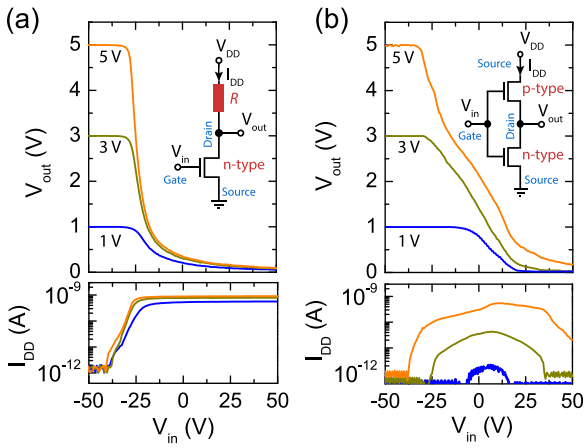

FIG. 3. (a) Output voltage, V_{out} (top panel), and supply current, I_{DD} (bottom panel), as a function of input voltage ($V_{in} = V_G$) for supply voltages, and V_{DD} of 1, 3, and 5 V, respectively. The inverter shows a maximum static current of ~1 nA with a stand-by current of ~1 pA. The circuit schematic of the inverter with load resistance, $R = 1.5$ GΩ, is shown in the inset. (b) Output voltage, V_{out} (top panel), and supply current, I_{DD} (bottom panel), as a function of input voltage ($V_{in} = V_G$) for supply voltages (V_{DD}) of 1, 3, and 5 V. The inset shows the inverter circuit obtained by replacing the load-resistance for the p-type transistor. The inverter shows a maximum driving current of ~1 nA for inversion and a steady state stand-by current of ~1 pA.

replace the load resistance by a p-type vertical transistor. As presented above, the CuPc-based transistor can be switched ON (OFF) for negative (positive) gate voltages. The circuit diagram for this inverter is displayed in the inset of Fig. 3(b). The top panel of Fig. 3(b) shows the full rail-to-rail transfer curves from V_{DD} to 0 V as in the previous case of Fig. 3(a). However, in this case, the supply current can be as low as ∼1 pA before and after the inversion, while it increases up to ∼1 nA during the inversion. This kind of complementary inverters with very low steady-state current would enable the exploration of more complex digital circuits based on hybrid graphene–organic heterostructures.

In conclusion, we have demonstrated an almost negligible barrier for charge carriers to completely overcome the thermionic-emission process in-between the graphene-electrode and the organic thin film. The transparent barrier is achieved in a vertical transistor architecture induced by the applied gate-voltages. The transistors provide a very low OFF-state current below ∼1 pA and a high ON-OFF current ratio reaching seven orders of magnitude for the graphene/PTCDI-C8 combination. We have investigated the effects of interface-limited and bulk-dominated transports on the electrical performance of these hybrid graphene-organic devices. We suggest that the bulk-dominated transport is the active mechanism when the graphene-organic interface energy barrier is lower than ∼0.2 eV. Finally, by assembling an n-type and a p-type vertical organic transistor, we demonstrate complementary inverters.

See supplementary material for details on device fabrication and transport analysis.

We acknowledge the financial support from the European Union 7th Framework Programme under the European Research Council (Grant No. 257654-SPINTROS), the Marie Curie Actions (607904-13-SPINOGRAPH), the Spanish Ministry of Economy under Project No. MAT2015-65159-R, Maria de Maeztu Units of Excellence Program-MDM-2016-0618, and the Basque Government under Project No. PC2015-1-01. A.A. thanks the Basque Government for the Ph.D. fellowship PRE 2015-2-0139.

The authors declare no conflict of interest.

[1]Y. Liu, N. O. Weiss, X. Duan, H.-C. Cheng, Y. Huang, and X. Duan, Nat. Rev. Mater. **1**, 16042 (2016).
[2]D. Jariwala, T. J. Marks, and M. C. Hersam, Nat. Mater. **16**, 170 (2017).
[3]C.-H. Kim and I. Kymissis, J. Mater. Chem. C **5**, 4598 (2017).
[4]L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, Appl. Phys. Lett. **88**, 083502 (2006).
[5]H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, Nature **445**, 745 (2007).
[6]H. Sirringhaus, N. Tessler, and R. H. Friend, Science **280**, 1741 (1998).
[7]M. G. Lemaitre, E. P. Donoghue, M. A. McCarthy, B. Liu, S. Tongay, B. Gila, P. Kumar, R. K. Singh, B. R. Appleton, and A. G. Rinzler, ACS Nano **6**, 9095 (2012).
[8]H. Hlaing, C. H. Kim, F. Carta, C. Y. Nam, R. A. Barton, N. Petrone, J. Hone, and I. Kymissis, Nano Lett. **15**, 69 (2015).
[9]S. Parui, L. Pietrobon, D. Ciudad, S. Vélez, X. Sun, F. Casanova, P. Stoliar, and L. E. Hueso, Adv. Funct. Mater. **25**, 2972 (2015).
[10]C.-J. Shih, R. Pfattner, Y.-C. Chiu, N. Liu, T. Lei, D. Kong, Y. Kim, H.-H. Chou, W.-G. Bae, and Z. Bao, Nano Lett. **15**, 7587 (2015).
[11]B. J. Kim, E. Hwang, M. S. Kang, and J. H. Cho, Adv. Mater. **27**, 5875 (2015).
[12]M. A. Baldo and S. R. Forrest, Phys. Rev. B **64**, 085201 (2001).
[13]N. B. Kotadiya, H. Lu, A. Mondal, Y. Ie, D. Andrienko, P. M. W. Blom, and G.-J. H. A. Wetzelaer, Nat. Mater. **17**, 329 (2018).
[14]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[15]Y.-J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, Nano Lett. **9**, 3430 (2009).
[16]H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim, Science **336**, 1140 (2012).
[17]S. Parui, M. Ribeiro, A. Atxabal, R. Llopis, F. Casanova, and L. E. Hueso, Nanoscale **9**, 10178 (2017).
[18]Z. Zhu, I. Murtaza, H. Meng, and W. Huang, RSC Adv. **7**, 17387 (2017).
[19]S. Vélez, D. Ciudad, J. Island, M. Buscema, O. Txoperena, S. Parui, G. A. Steele, F. Casanova, H. S. J. van der Zant, A. Castellanos-Gomez, and L. E. Hueso, Nanoscale **7**, 15442 (2015).
[20]P. W. M. Blom, M. J. M. de Jong, and J. J. M. Vleggaar, Appl. Phys. Lett. **68**, 3308 (1996).
[21]P. S. Davids, I. H. Campbell, and D. L. Smith, J. Appl. Phys. **82**, 6319 (1997).
[22]J. Frenkel, Phys. Rev. **54**, 647 (1938).
[23]K. Berke, S. Tongay, M. A. McCarthy, A. G. Rinzler, B. R. Appleton, and A. F. Hebard, J. Phys. Condens. Matter **24**, 255802 (2012).
[24]J. S. Kim, B. J. Kim, Y. J. Choi, M. H. Lee, M. S. Kang, and J. H. Cho, Adv. Mater. **28**, 4803 (2016).