Three-terminal resistive switching memory in a transparent vertical-configuration device

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Three-terminal resistive switching memory in a transparent vertical-configuration device

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The resistive switching phenomenon has attracted much attention recently for memory applications. It describes the reversible change in the resistance of a dielectric between two non-volatile states by the application of electrical pulses. Typical resistive switching memories are two-terminal devices formed by an oxide layer placed between two metal electrodes. Here, we report on the fabrication and operation of a three-terminal resistive switching memory that works as a reconfigurable logic component and offers an increased logic density on chip. The three-terminal memory device we present is transparent and could be further incorporated in transparent computing electronic technologies. © *2014 AIP Publishing LLC*.
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The storage-devices market is under an ever-increasing need to design a new type of non-volatile memory that would successfully replace the low write speed and low endurance Flash memory. Recently, resistive random access memories (ReRAM) based on resistive switching (RS) in oxide thin films have been shown to be exceptional candidates for the next generation of non-volatile storage devices.[1,2] RS systems have in general a simple metal-oxide-metal structure in which the state of the oxide can be reversibly varied between a low resistance (LR) and a high resistance (HR) state by the application of electrical pulses between the two metallic terminals. Despite such simple structure, ReRAMs have been proven to work fast, with switching times of 10 ns, and to be reliable, with an endurance of 10^{12} processing cycles.[2] Additionally, the RS effect is ubiquitous and has been demonstrated in many materials, including many binary and ternary oxides.[3–7] Expanding from simple memory devices, numerous other applications have been proposed for ReRAMs, such as in neuromorphic systems or high performance computing.[8–16]

A non-volatile aluminium oxide (Al_2O_3) ReRAM controlled both by the voltage applied between the electrodes and by the light irradiated on the devices has been previously reported, together with possible applications in modelling bio-inspired processes.[7,16] A drawback of the light-controlled memory devices is the difficulty to incorporate a light-source on chip. In the device that we present in this current article, we replace the light irradiation as extra-control parameter by a third, gate, electrode that is incorporated on chip. We show that this gate electrode can modulate the current flowing between the source-drain electrodes that are conventionally used to contact the ReRAM oxide film. Our three-terminal device has a vertical configuration with the same footprint area as a two-terminal device, and hence implementing further functionalities without requesting extra wafer area.

The device is based on the RS in Al_2O_3 dielectric films and has indium tin oxide (ITO) as material for the electrical metallic contacts. Our system expands from a typical binary memory element and operates as a reconfigurable logic element. In general terms, a reconfigurable logic element is a programmable logic hardware that can change its functionality or value during operation and normally comprises several diverse components connected together.[11,14] The three-terminal device we fabricate could alone replace the function of such multi-component system. Moreover, the reconfigured state is retained even in the absence of any applied voltage or current since the incorporated RS memory is non-volatile. Additionally, our design is within a transparent, all-oxide device. Transparent electronics is one of the emerging technologies for the next generation of electronic systems, bringing, for example, transparent displays, or transparent information storage.[17–21]

The fabrication of the devices begins with the preparation of ITO bars by photolithography and sputtering on a Pyrex-glass substrate. These bars operate as gate electrodes (A in Figs. 1(a) and 1(b)). In the next step, we grow a 5-nm thick SiO_2 film by sputtering (B in Fig. 1). The thickness of the SiO_2 layer was optimized to 5 nm. Thinner layers seem not to be continuous or to be leaky, while thicker layers need higher power consumption and may present the phenomenon of resistive switching themselves.[22] The SiO_2 tunnel barrier film separates the gate electrode and the ITO source electrode deposited afterwards (C in Fig. 1).[23] These source electrodes form a crossbar with the gate electrode, and are 100 μm wide and 1 cm long as defined by photolithography. Subsequently, we grow a 50-nm thick Al_2O_3 film by atomic layer deposition as RS memory layer (D in Fig. 1). On top of the Al_2O_3 and on the crossbar intersecting parts, we prepare 100 μm by 100 μm ITO top contacts as drain electrodes (E in Fig. 1). The thickness of the ITO is 50 nm for each of the three electrodes.

Current-voltage (I-V) characteristics were measured at room temperature with a two channels source-meter in a three-probe configuration. We apply a voltage V between the source and the drain electrodes (C–E in Fig. 1) that are in direct contact with the Al_2O_3 memory layer. At the same time, we apply an additional gate voltage V_g on the gate electrode (A in Fig. 1), so there are two inputs connected to

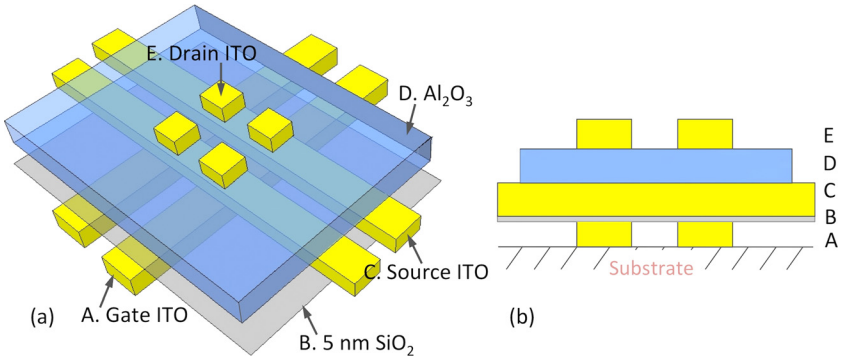

FIG. 1. (a) Device sketch presenting the order in configuration of the three-terminal devices. The different layers (from bottom to top) are the gate ITO bar-shaped electrodes (A), the insulating SiO_2 film (B), the ITO source electrodes (C), the Al_2O_3 resistive switching memory layer (D), and finally the ITO drain top contacts (E). (b) Schematic cross-section of the device, showing the layers with the same legend as in panel (a).

our device as in a standard transistor operation. In Fig. 2, we show typical I-V curves obtained with gate voltages in the range from 0 to 10 V. The I-V curve obtained for $V_g = 0$ V is equivalent to that of a conventional two-terminal ReRAM. Ramping the voltage from 0 V to +18 V and then returning to a lower V, the current presents a clear hysteretic behaviour as the current is lower in the returning branch of the loop. The device can be brought back to the initial state by the application of a negative voltage (V = −18 V, in the specific case depicted) and then returning back to 0 V. The application of a voltage V of +18 V to the device brings the system in the HR state from the pristine LR state, while the reverse bias of −18 V recovers the LR state. For information storage, we exploit the hysteresis present on the current-voltage curves in forward bias.[7] The I-V curves can be repeated under the application of different gate voltages (Fig. 2(a)). In general terms, a higher voltage on the gate electrode leads to a lower source-drain current measured and to a smaller hysteretic memory window in forward bias. We prove here that we can control the device behaviour by using the third gate terminal, adding an extra degree of freedom as compared with conventional RS memory devices. The behavior of the device presented in this paper was accurately reproduced on the five other tested devices prepared following the same recipe. In Figs. 2(b) and 2(c), we show that a positive V_g applied on the gate electrode (A in Fig. 1) decreases the source-drain (C-E) current magnitude in forward bias while increasing it in reverse bias, which is understandable since the gate voltage is added to the source voltage.

The vertical design that we propose for our three-terminal device is possible due to the electron-mediated conduction in Al_2O_3.[7,24] In forward source-drain voltage bias, a depletion region is generated at the source ITO–Al_2O_3 interface. Electrons from ITO (C in Fig. 1) are injected in the Al_2O_3 layer when the electric field is high enough to overcome this energy barrier and are then transported to the top drain electrode (E in Fig. 1) when a positive voltage higher than a threshold value is applied to this top electrode. Some of the electrons passing between the source and the drain are trapped in the Al_2O_3 layer situated in between, changing its resistance from a LR state to a HR state, so a memory operation mode is possible. The transition from HR to LR occurs when trapped charges are gradually removed by a negative applied voltage. When a positive voltage is applied to the gate electrode (A in Fig. 1), some electrons from the source are redirected towards this most-bottom electrode instead of the top drain electrode. As a result, the current reaching the top electrode is reduced in forward bias, which is the voltage window we operate our memory in. This means that the modulation of the source-drain current between various states is possible with the gate electrode.

To further probe the effect of the change in the applied gate voltage on the current passing through the ReRAM, we performed I-V loops while changing V_g during the loop (Figs. 3(a) and 3(b)). In Fig. 3(a), we display an I-V curve measured by sweeping the voltage V from 0 V to −18 V and then back to 12.5 V with a gate voltage V_g of 6 V continuously applied. When we reach 12.5 V, we keep on measuring the I-V curve, but at that specific point, we change the gate voltage from 6 V to 0 V. Then we maintain V_g at 0 V while continuing to sweep V from 12.5 V to 18 V and then back to 0 V. The same measuring scheme applies for Fig. 3(b), just that in this case at 12.5 V, we change the gate voltage from 0 V to 6 V. We observe that a sudden change in the gate

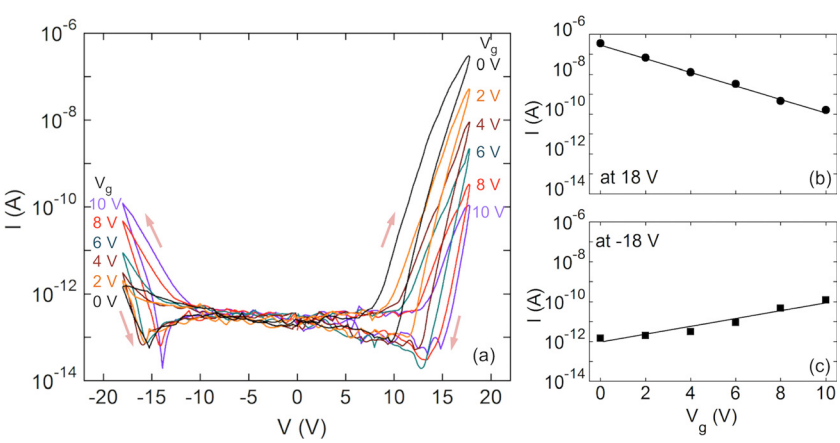

FIG. 2. (a) Current (I)–voltage (V) characteristics measured with gate voltages in the range from 0 V to 10 V. The arrows indicate the direction of the voltage sweep. During the I-V curves measurements, the gate voltage V_g was continuously applied. The dependence of the current measured at 18 V or −18 V on the gate voltage is presented in (b) and (c), respectively. We see that V_g has opposite effects for opposite polarities of V, since it increases the magnitude of the current for negative voltages and decreases it for positive voltages applied between the source and the drain electrodes.

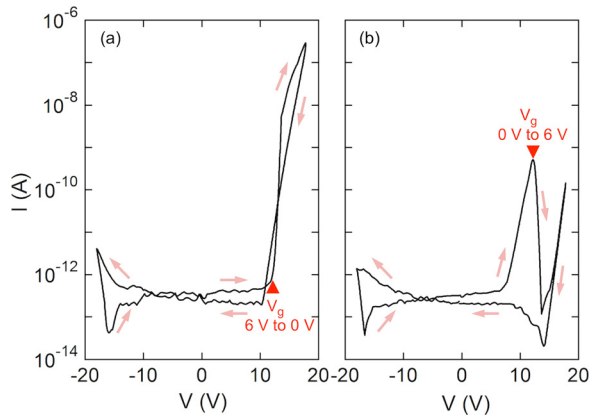

FIG. 3. Source-drain current change when changing the gate voltage at a fixed time instant. (a) The I-V curve is measured by sweeping V from 0 V to −18 V and back to 12.5 V with a V_g of 6 V continuously applied. When reaching 12.5 V, we continue measuring the I-V curve, but at this instant (marked in the figure by a triangle), we change the gate voltage from 6 V to 0 V and we keep V_g 0 V while sweeping V to 18 V then back to 0 V. (b) The I-V curve is measured by sweeping V from 0 V to −18 V and back to 12.5 V with no V_g applied. When reaching 12.5 V, we continue measuring the I-V curve, but at this time instant (marked with a triangle), we change the gate voltage from 0 V to 6 V and we keep V_g 6 V while sweeping V to 18 V then back to 0 V.

voltage, as in the 12.5 V points indicated in Figs. 3(a) and 3(b), has a rapid and dramatic effect on the current flowing between the other two electrodes connecting the Al_2O_3 memory layer. In the case of Fig. 3(a), the change of V_g from 6 V to 0 V in the indicated point V = 12.5 V is equivalent to an abrupt increase in the current from the 10^{-12} A range to the 10^{-9} A range. For Fig. 3(b) case, the change of V_g from 0 V to 6 V in the indicated point V = 12.5 V is equivalent to a sudden decrease in the current from the 10^{-10} A range to the 10^{-13} A range. These results prove that the third electrode offers a reliable extra control parameter for the current flowing through the memory device.

We verified that our reconfigurable logic element can be set into various stable states depending on V_g and that it keeps its configured state in the absence of power supply by remnant current measurements, displayed in Fig. 4 and by data retention measurements, shown in Fig. 5.

In Fig. 4(a), we present the remnant current hysteresis loops obtained after writing in the presence of different applied gate voltages. The remnant current I_{rem} loops are acquired point by point.[7,16,25] Each point of the loops represents the remnant current measured after the following two operations: first we apply a writing voltage pulse V_{write} together with the gate voltage V_g indicated in Fig. 4(a) and second, we wait a 100 ms time at 0 V to discharge capacitive effects and prove the memory non-volatility. After the waiting time at 0 V, we measure the remnant current I_{rem} with a read-voltage V_{read} = 12 V, and with no applied V_g.[7,25] The 12 V value for the reading voltage was selected as to be in the hysteretic region of the I-V curves (Fig. 2) and to be lower than 18 V, which is the voltage used to write the memory. The current-voltage characteristics (Fig. 2) and the remnant current hysteresis loops (Fig. 4(a)) are expected to be very different since they are obtained in dissimilar processes. The I-V curves are obtained by continuously measuring the current at different voltages. The data presented in Fig. 4(a) show the remnant current measured with the same V_{read} for all the points, which means that we probe in same conditions the state kept by the memory element 100 ms after writing the data in different conditions (different $V_{write} + V_g$). We can observe that the gate voltage applied only during the writing step has a significant effect on the remnant current I_{rem} measured 100 ms later with no applied gate-voltage. This proves that the gate electrode efficiently modulates the state retained by the memory. In Figs. 4(b) and 4(c), we present the remnant current values measured at 12 V without V_g after applying a V_{write} of 18 V or −18 V together with a gate voltage, immediately followed by 100 ms waiting time in order to remove the capacitive effects and to prove non-volatility. We observe that by increasing V_g during writing the remnant current measured without V_g increases, confirming that the effect of a previous application of a gate voltage is remembered accordingly.

To further probe the non-volatility of the configured data, we performed data-retention experiments (see Fig. 5). For the retention curves presented in Fig. 5(a), we applied at time 0 one writing voltage pulse of −18 V for reaching the LR state together with a V_g of 0 V in this particular case. Then we performed 60 consecutive readings of the remnant current every 10 s with 12 V pulses and without any gate voltage. After this, we applied one writing voltage pulse of 18 V for reaching the HR state, together with a V_g of 0 V. Then we again performed 60 consecutive readings of the remnant current every 10 s with 12 V, without V_g. We can clearly see in Fig. 5(a) that the LR and HR states, even if read with the same voltage of 12 V, are well defined and separated from each other, as expected for non-volatile memory

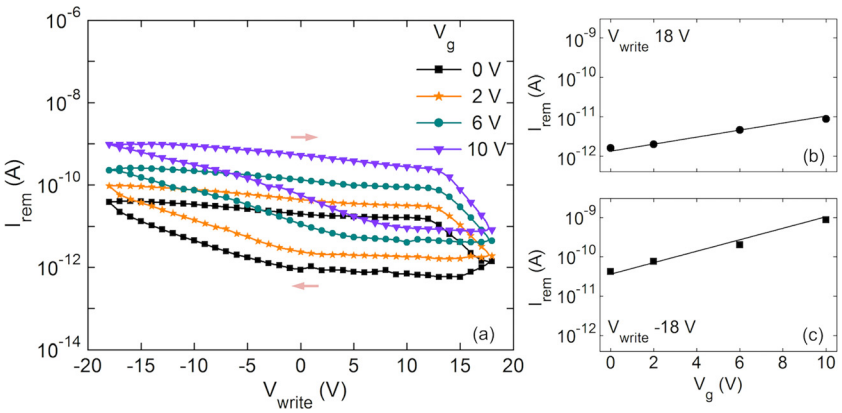

FIG. 4. (a) Remnant current hysteresis loops. In each point, I_{rem} was measured at 12 V without any gate voltage V_g, after applying a V_{write} together with a V_g, immediately followed by a waiting time of 100 ms at 0 V. The arrows indicate the direction in which the curves are measured. The remnant current read at 12 V after writing the memory at 18 V or −18 V is presented in (b) and (c), respectively. Each data point in (b) and (c) is the result of writing at 18 V or −18 V, followed by 100 ms at 0 V, and then reading of I_{rem} at 12 V to obtain the non-volatile memory state.

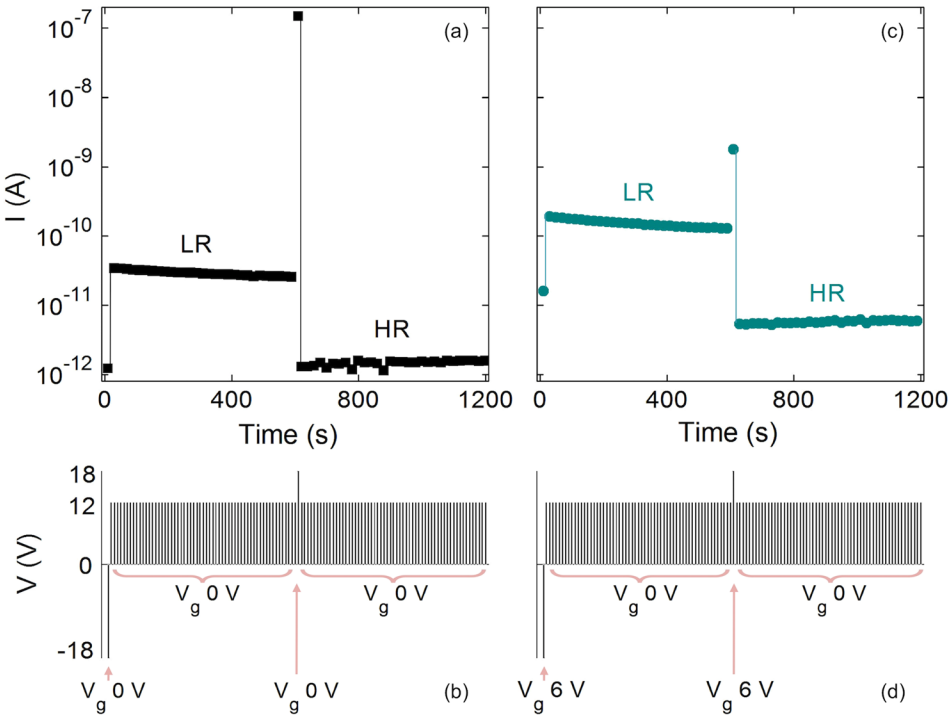

FIG. 5. Data retention measurements. (a) Data retention measurements obtained with reading pulses of 12 V, without applied gate voltage. The consecutive reading steps are performed after we set the system in a LR or HR state by a writing voltage pulse of −18 V or 18 V, applied together with a gate voltage of 0 V in this case. (b) The voltage pulses sequence applied for obtaining the data presented in (a) are displayed. (c) Data retention verified by readings at 12 V with no applied V_g after setting the system in a LR or HR state by one −18 V or 18 V writing voltage pulse accompanied by a gate voltage of 6 V. (d) The sequence of voltage pulses applied for obtaining the data presented in (c) is sketched.

devices. The corresponding voltages applied for the data presented in Fig. 5(a) are sketched in Fig. 5(b). A similar process to that shown in Fig. 5(a) is indicated in Fig. 5(c), although in this case the writing steps with −18 V and 18 V are accompanied by a gate voltage V_g of 6 V. The consecutive readings of the retained data are again performed with voltage pulses of 12 V and no additional V_g. All the reading steps in Figs. 5(a) and 5(c) are performed under the same conditions and only the two writing steps are different. The corresponding voltages applied for the data presented in Fig. 5(c) are displayed in Fig. 5(d). The duration of each applied pulse for writing or reading is 20 ms. The LR and HR states in (c), for which a V_g of 6 V was applied during writing, are different than the LR and HR levels in (a), for which V_g was 0 V during writing. The information retained over time by our memory depends on the gate voltage applied during the writing steps, the information is remembered accordingly to the modulating V_g.

One possible application for the devices here presented is as a reconfigurable logic element, which is programmable logic hardware that can change its functionality or value during operation, as presented above. Another application that can be foreseen for such devices is in neuromorphic systems, whose design and function are based on neurobiology. The resistive memories present some key aspects of synapses in the brain, since the voltage pulses applied between the two electrodes act like the neuronal action potentials. These action potentials change the synaptic weight (or strength) in biological learning processes. In our three-terminal device, the electrical resistance (which is equivalent to the synaptic weight) is modulated not only by the source-drain voltage (equivalent to neuronal action potentials) as in conventional ReRAMs but also by the gate voltage (acting as neuromodulator, present in many brain processes).[16]

In conclusion, we introduced a three-terminal ReRAM device in which the state of the memory device can be modulated via the application of a voltage on the third, gating electrode. Non-volatile states can be effectively set in the device by using different gate voltages, offering an extra control parameter for ReRAMs, in addition to the top-bottom controlling electrodes found in conventional two-terminal devices. Our solid-state device can become a tool for programmable logics or for simulation of complex neuronal operations. The device is formed of all-oxide transparent components, offering this system to advanced future applications in transparent electronics products.

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